

Description:

TEKQ TSD133XXX is a new 133X Super Fast Performance mass-storage system based on innovations in semiconductor technology which designed in advanced SD specification Ver.1.1. It's a special design for high performance of data transformation for SD Card system standard define in the SD card System specification which including telecommunication, audio, video, computer and electronic devices.

Features:

- **Capacity: 256MB / 512MB / 1GB / 2GB**
- **Form Factor: 24mm x 32mm x 2.1mm**
- **Voltage range : 2.7 - 3.6V**
- **Operating Temperature: -25 ~ 85°C**
- **Maximum Data Transfer Rate: 20MB/sec**
- **Designed for read-only and read/write cards**
- **Fully compatible with SD card spec. v1.1**
- **Copyrights Protection Mechanism - Complies with highest security of SDMI standard**
- **Mechanical Write Protection Switch**
- **Forward compatibility to Multi Media Card**
- **Supports Copy Protection for Recorded Media(CPRM) for music and other commercial media**
- **Low power consumption : automatic power down and automatic wake up, smart power management**
- **No external programming voltage required**

Functional Descriptions

Fig. 1-1 shows the SD memory card system diagram.

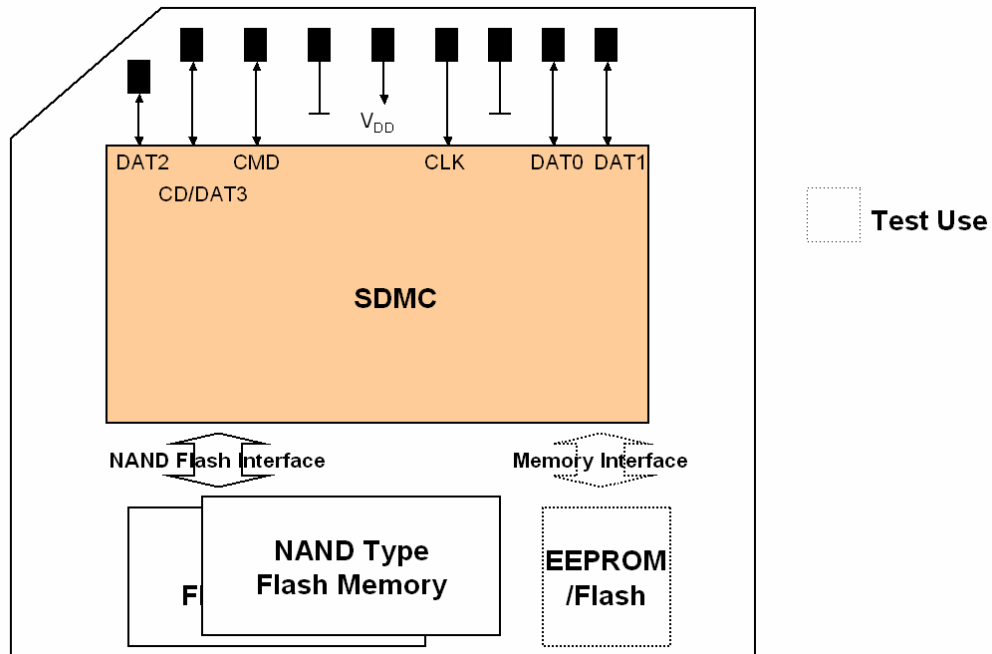


Fig. 1-1 SD memory card system diagram

1.1 Flash Memory Management and Power Control

The SD Memory Card contains a high level, intelligent subsystem that provides many capabilities including:

- Host independence from details of erasing and programming flash memories
- Management of flash memory defects
- Management of error recovery including a powerful error correction code (ECC)
- Power management for low power operation

1.1.1 Flash Memory Access

To write or read a sector (or multiple sectors), the master (host device) simply issues a read or a write command set to the SD Memory Card. The command set contains the address and related information about the access characteristics. The master (host device) does not get involved in the details of how the flash memory is erased, programmed or read.

1.1.2 Management of flash memory defects

The SD Memory Card also contains a sophisticated defect and error management system. The SD Memory Card does a read after write under margin conditions to verify that the data is written correctly (except in the case of write pre-erased sectors). In case that a bit is found to be defective, the SD Memory Card replaces this bad bit with a spare bit within the sector header. If necessary, the SD Memory Card will even replace the entire sector with a spare sector. This is completely transparent to the master (host device) and does not consume any user data space.

1.1.3 Error Recovery

In the rare case a read error does occur, the SD Memory Card has an innovative algorithm to recover the data. The last line of defense is to employ a powerful ECC to correct the data. If ECC is used to recover data, defective bits are replaced with spare bits to ensure they do not cause any future problems.

1.1.4 Power Management

A power saving feature of the SD Memory Card is automatic entrance and exit from sleep mode. Upon completion of an operation, the SD Memory Card will enter the sleep mode to conserve power if no further commands are received within X seconds, where X is programmable by software. The master does not have to take any action for this to occur. The SD Memory Card is in sleep mode except when the host is accessing it, thus conserving power.

Any command issued by the master to the SD Memory Card will cause it to exit sleep mode and response to the master.

1.2 SD Memory Card Interface

The SD Memory Card provides two alternative communication protocols: SD and SPI. Applications can choose either one of modes. Mode selection is transparent to the hosts. The SD Memory Card automatically detects the mode of the reset command and

will expect all further communication to be in the same communication mode. Therefore, applications that use only one communication mode do not have to be aware of the other.

1.3 Content Protection for Recordable Media

The Content Protection for Recordable Media (CPRM) technology is designed to meet the following criteria:

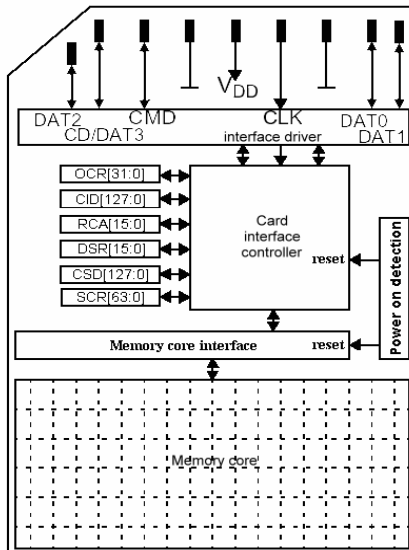
- It meets the content owners' requirements for robustness and system renewability
- It is applicable for both audio and video content
- It is equally suitable for implementation on PCs and CE devices
- It is applicable to different media type

The system is based on the following technical elements

- Key management for interchangeable media
- Content encryption
- Media based renewability

2. Interface and Pin descriptions

SD Memory Card architecture Diagram



Pin #	SD Mode			SPI Mode		
	Name	Type	Description	Name	Type	Description
1	CD/DAT3	I/O/PP	Card Detect/Data Line [Bit3]	CS	I	Chip Select (neg true)
2	CMD	PP	Command/Response	DI	I	Data In
3	Vss1	S	Supply voltage ground	Vss1	S	Supply voltage ground
4	Vdd	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	
6	Vss2	S	Supply voltage ground	Vss2	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line [Bit1]	RSV		
9	DAT2	I/O/PP	Data Line [Bit2]	RSV		

- 1) S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers;
- 2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate

as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to MultiMediaCards.

- 3) After power up this line is input with 50KOhm pull-up (can be used for card detection or SPI mode selection). The pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V _{CC}	Power supply relative to V _{SS}	2.5 to 4.0	V
V _{IN}	Input voltage relative to V _{SS}	-0.3 to 4.0	V
T _{STG}	Storage temperature	-40 to 85	°C
T _{OP}	Operation temperature	-25 to 85	°C

Table 3-1 Absolute Maximum Ratings Parameter Value

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the optional sections of this datasheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

3.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V _{CC}	Power supply voltage	2.7	3.3	3.9	V
V _{SS}	Power supply voltage	0	0	0	V
T _J	Junction operation temperature	0	-	85	°C
T _A	Recommended operating ambient temperature	0	-	85	°C

Table 3-2 Recommended Operating Conditions Parameter Value

3.3 Capacitance

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNTIS
C_{IN}	Input capacitance			2.2		pF
C_{OUT}	Output capacitance			2.2		pF
C_{BID}	Bi-directional buffer capacitance			2.2		pF
R_{DAT3}	Pull up resistance inside xb_data_sd[3]		10	75	90	K Ohm

Table 3-3 Capacitance Parameter Value

Note: The capacitance listed above does not include package capacitance.

3.4 DC Characteristics

Symbol	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input low voltage		$V_{SS} - 0.3$		$0.25V_{CC}$	V
V_{IH}	Input high voltage		$0.625V_{CC}$		$V_{CC} + 0.3$	V
V_{OL}	Output low voltage	$I_{OL} = 100\mu A @ V_{CC_min}$			$0.125V_{CC}$	V
V_{OH}	Output high voltage	$I_{OH} = -100\mu A @ V_{CC_min}$	$0.75V_{CC}$			V
I_{IN}	Input leakage current	$V_{IN} = V_{CC} \text{ or } 0$	-10	+/- 1	10	μA
I_{OUT}	Tri-state output leakage current		-10	+/- 1	10	μA
I_{STBY}	Standby current	3.3V@clock stop		0.3	0.6	mA
I_{OP}	Operation current	3.3V@25MHz (Write)		15	25	mA
		3.3V@25MHz (Read)		15	25	mA
I_{OP}	Operation current	3.3V@50MHz (Write)		30	45	mA
		3.3V@50MHz (Read)		30	45	mA

Table 3-4 DC Characteristics Parameter Value

3.5 AC Characteristic

3.5.1 Bus Timing (Default Mode)

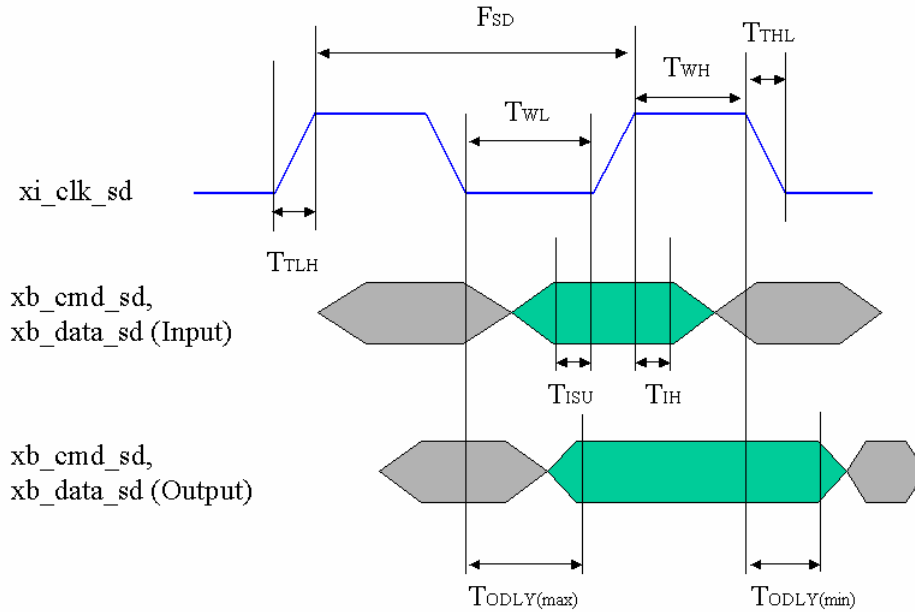
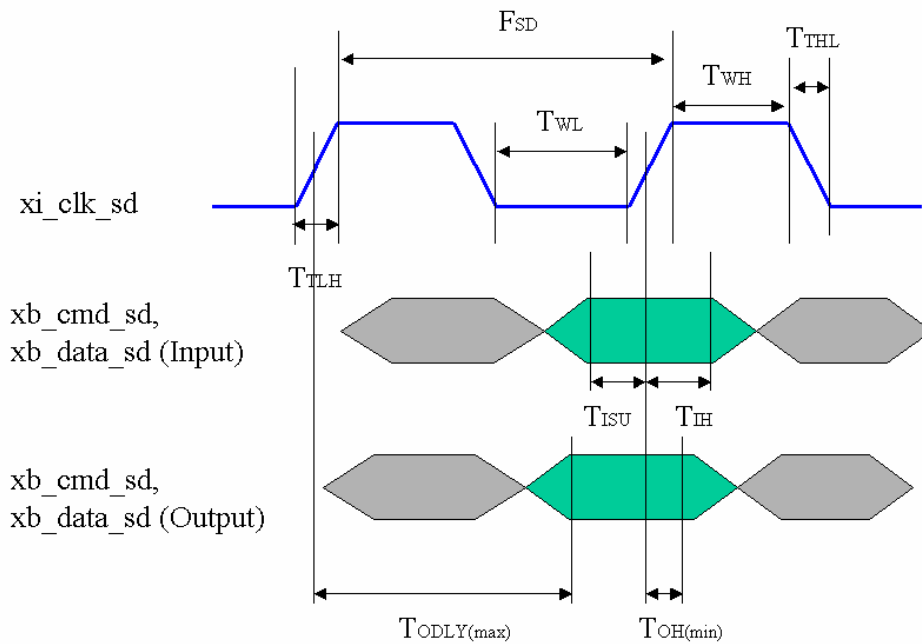


Fig. 3-1 Timing Diagram of Default Mode Bus Timing

SYMBOL	PARAMETER	MIN	MAX	UNIT	Note
F_{SD}	SD clock frequency	0	25	MHz	
t_{WL}	Clock low time	10		ns	
t_{WH}	Clock high time	10		ns	
t_{TLH}	Clock rise time		10	ns	
t_{THL}	Clock fall time		10	ns	
t_{ISU}	Input setup time	5		ns	
t_{IH}	Input hold time	5		ns	
t_{ODLY}	Output delay time	0	14	ns	

Table 3-5 Default Mode Bus Timing Parameter Value

3.5.2 Bus Timing (High-speed Mode)



Signal	I/O	Source/Destination	Description	Comment
xi_clk_sd	I	SDSC	SD host clock input.	SD CLK
xb_cmd_sd	I/O	SDSC	SD host command/response in the SD mode. DataIn in the SPI mode.	SD CMD, SPI DI
$xb_data_sd[0]$	I/O	SDSC	SD host data input/output line 0. Data output in the SPI mode.	SD DAT0
$xb_data_sd[2:1]$	I/O	SDSC	SD host data input/output line 1 and 2.	SD DAT1, SD DAT2
$xb_data_sd[3]$	I/O	SDSC	SD host data input/output line 3 in the SD mode. CS in the SPI mode.	SD DAT3, SPI CS

Fig. 3-2 Timing Diagram of High-Speed Mode Bus Timing

SYMBOL	PARAMETER	MIN	MAX	UNIT	Note
F_{SD}	SD clock frequency	0	50	MHz	
t_{WL}	Clock low time	7		ns	
t_{WH}	Clock high time	7		ns	
t_{TLH}	Clock rise time		3	ns	
t_{THL}	Clock fall time		3	ns	
t_{ISU}	Input setup time	6		ns	
t_{IH}	Input hold time	2		ns	
t_{ODLY}	Output delay time		14	ns	
t_{OH}	Output hold time	2.5		ns	

Table 3-3 High-Speed Mode Bus Timing Parameter Value