

## **Description:**

TCF80XXX Compact Flash Card (CF) is upgrade version of Ultra High Speed flash card, it is low power consumption construct with Nand Flash type memory solution device with ATA interface by operates in both 5V and 3.3V power supplies. It is a perfect choice of solid-state mass-storage cards for battery backup handheld devices such as Digital Camera, Audio Player, PDA, or the applications which require large capacity.

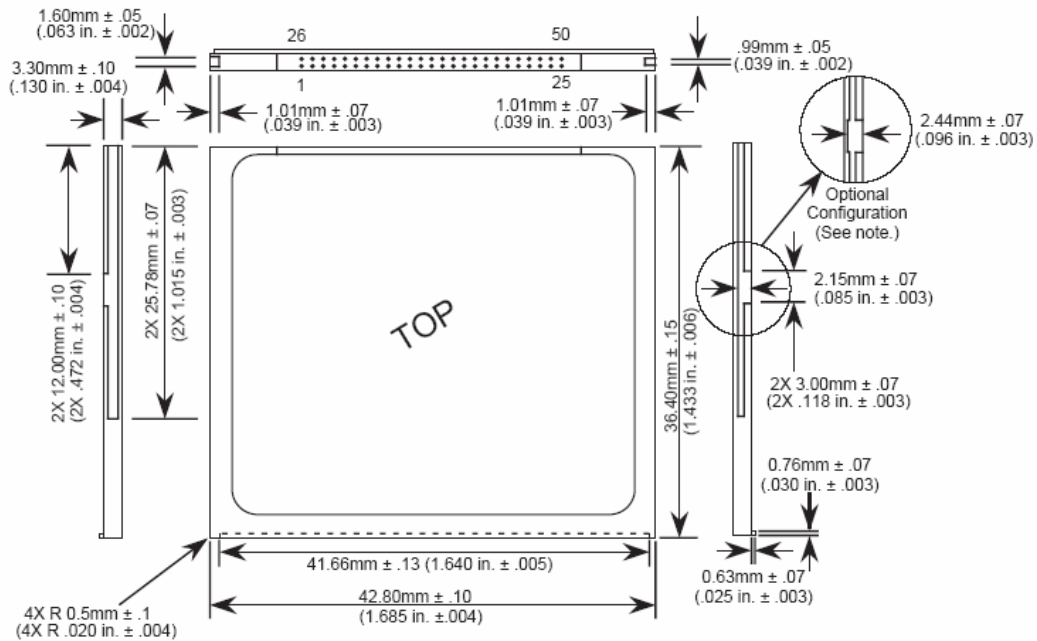
## **Features:**

- Capacity: 128MB / 256MB / 512MB / 1GB / 2GB / 4GB
- Form Factor: 36.4mm x 42.8mm x 3.3mm
- Voltage range : 3.3V - 5V
- Operating Temperature: 0 ~ 70°C
- Storage Temperature: -20 ~ 80°C
- Maximum Data Transfer Rate up to 12MB/sec
- Support 8bit / 16 bit data transfer on host data bus
- Embedded with data error correction
- Support PC card ATA and True IDE interface
- Low power consumption
- No external programming voltage required

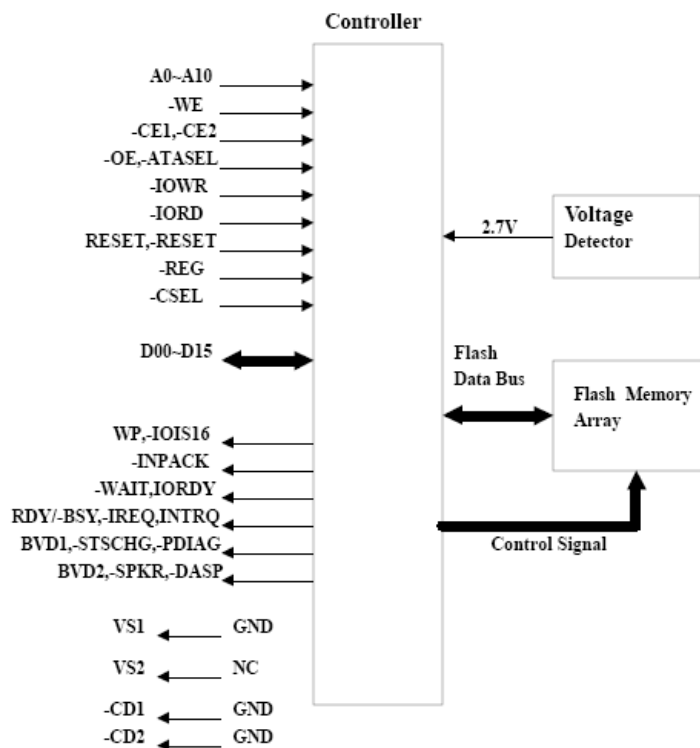
# Compact Flash Card

(TCF80XXX)  
TEKQ International

## Block Diagram:



Note: The optional notched configuration was shown in the CF Specification Rev. 1.0. In specification Rev. 1.2, the notch was removed for ease of tooling. This optional configuration can be used but it is not recommended.



# Compact Flash Card

(TCF80XXX)

TEKQ International

## Ping Assignments and Pin Type:

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode <sup>4</sup>			
Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type
1	GND		Ground	1	GND		Ground	1	GND		Ground
2	D03	I/O	I1Z, OZ3	2	D03	I/O	I1Z, OZ3	2	D03	I/O	I1Z, OZ3
3	D04	I/O	I1Z, OZ3	3	D04	I/O	I1Z, OZ3	3	D04	I/O	I1Z, OZ3
4	D05	I/O	I1Z, OZ3	4	D05	I/O	I1Z, OZ3	4	D05	I/O	I1Z, OZ3
5	D06	I/O	I1Z, OZ3	5	D06	I/O	I1Z, OZ3	5	D06	I/O	I1Z, OZ3
6	D07	I/O	I1Z, OZ3	6	D07	I/O	I1Z, OZ3	6	D07	I/O	I1Z, OZ3
7	-CE1	I	I3U	7	-CE1	I	I3U	7	-CS0	I	I3Z
8	A10	I	I1Z	8	A10	I	I1Z	8	A10 <sup>2</sup>	I	I1Z
9	-OE	I	I3U	9	-OE	I	I3U	9	-ATA SEL	I	I3U
10	A09	I	I1Z	10	A09	I	I1Z	10	A09 <sup>2</sup>	I	I1Z
11	A08	I	I1Z	11	A08	I	I1Z	11	A08 <sup>2</sup>	I	I1Z
12	A07	I	I1Z	12	A07	I	I1Z	12	A07 <sup>2</sup>	I	I1Z
13	VCC		Power	13	VCC		Power	13	VCC		Power
14	A06	I	I1Z	14	A06	I	I1Z	14	A06 <sup>2</sup>	I	I1Z
15	A05	I	I1Z	15	A05	I	I1Z	15	A05 <sup>2</sup>	I	I1Z
16	A04	I	I1Z	16	A04	I	I1Z	16	A04 <sup>2</sup>	I	I1Z
17	A03	I	I1Z	17	A03	I	I1Z	17	A03 <sup>2</sup>	I	I1Z
18	A02	I	I1Z	18	A02	I	I1Z	18	A02	I	I1Z
19	A01	I	I1Z	19	A01	I	I1Z	19	A01	I	I1Z
20	A00	I	I1Z	20	A00	I	I1Z	20	A00	I	I1Z
21	D00	I/O	I1Z, OZ3	21	D00	I/O	I1Z, OZ3	21	D00	I/O	I1Z, OZ3
22	D01	I/O	I1Z, OZ3	22	D01	I/O	I1Z, OZ3	22	D01	I/O	I1Z, OZ3
23	D02	I/O	I1Z, OZ3	23	D02	I/O	I1Z, OZ3	23	D02	I/O	I1Z, OZ3
24	WP	O	OT3	24	-IOIS16	O	OT3	24	-IOCS16	O	ON3
25	-CD2	O	Ground	25	-CD2	O	Ground	25	-CD2	O	Ground
26	-CD1	O	Ground	26	-CD1	O	Ground	26	-CD1	O	Ground
27	D11 <sup>1</sup>	I/O	I1Z, OZ3	27	D11 <sup>1</sup>	I/O	I1Z, OZ3	27	D11 <sup>1</sup>	I/O	I1Z, OZ3
28	D12 <sup>1</sup>	I/O	I1Z, OZ3	28	D12 <sup>1</sup>	I/O	I1Z, OZ3	28	D12 <sup>1</sup>	I/O	I1Z, OZ3
29	D13 <sup>1</sup>	I/O	I1Z, OZ3	29	D13 <sup>1</sup>	I/O	I1Z, OZ3	29	D13 <sup>1</sup>	I/O	I1Z, OZ3
30	D14 <sup>1</sup>	I/O	I1Z, OZ3	30	D14 <sup>1</sup>	I/O	I1Z, OZ3	30	D14 <sup>1</sup>	I/O	I1Z, OZ3
31	D15 <sup>1</sup>	I/O	I1Z, OZ3	31	D15 <sup>1</sup>	I/O	I1Z, OZ3	31	D15 <sup>1</sup>	I/O	I1Z, OZ3
32	-CE2 <sup>1</sup>	I	I3U	32	-CE2 <sup>1</sup>	I	I3U	32	-CS1 <sup>1</sup>	I	I3Z
33	-VS1	O	Ground	33	-VS1	O	Ground	33	-VS1	O	Ground
34	-IORD	I	I3U	34	-IORD	I	I3U	34	-IORD <sup>7</sup>	I	I3Z
									HSTROBE <sup>8</sup>		
									-HDMARDY <sup>9</sup>		

# Compact Flash Card

(TCF80XXX)

TEKQ International

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode <sup>4</sup>			
Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type	Pin Num	Signal Name	Pin Type	In, Out Type
35	-IOWR	I	I3U	35	-IOWR	I	I3U	35	-IOWR <sup>7</sup>	I	I3Z
									STOP <sup>8,9</sup>		
36	-WE	I	I3U	36	-WE	I	I3U	36	-WE <sup>3</sup>	I	I3U
37	READY	O	OT1	37	-IREQ	O	OT1	37	INTRQ	O	OZ1
38	VCC		Power	38	VCC		Power	38	VCC		Power
39	-CSEL <sup>5</sup>	I	I2Z	39	-CSEL <sup>5</sup>	I	I2Z	39	-CSEL	I	I2U
40	-VS2	O	OPEN	40	-VS2	O	OPEN	40	-VS2	O	OPEN
41	RESET	I	I2Z	41	RESET	I	I2Z	41	-RESET	I	I2Z
42	-WAIT	O	OT1	42	-WAIT	O	OT1	42	IORDY <sup>7</sup>	O	ON1
									-DDMARDY <sup>8</sup>		
									DSTROBE <sup>9</sup>		
43	-INPACK	O	OT1	43	-INPACK	O	OT1	43	DMARQ	O	OZ1
44	-REG	I	I3U	44	-REG	I	I3U	44	-DMACK <sup>6</sup>	I	I3U
45	BVD2	O	OT1	45	-SPKR	O	OT1	45	-DASP	I/O	I1U, ON1
46	BVD1	O	OT1	46	-STSCHG	O	OT1	46	-PDIAG	I/O	I1U, ON1
47	D08 <sup>1</sup>	I/O	I1Z, OZ3	47	D08 <sup>1</sup>	I/O	I1Z, OZ3	47	D08 <sup>1</sup>	I/O	I1Z, OZ3
48	D09 <sup>1</sup>	I/O	I1Z, OZ3	48	D09 <sup>1</sup>	I/O	I1Z, OZ3	48	D09 <sup>1</sup>	I/O	I1Z, OZ3
49	D10 <sup>1</sup>	I/O	I1Z, OZ3	49	D10 <sup>1</sup>	I/O	I1Z, OZ3	49	D10 <sup>1</sup>	I/O	I1Z, OZ3
50	GND		Ground	50	GND		Ground	50	GND		Ground

Note: 1) These signals are required only for 16 bit accesses and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current.

2) The signal should be grounded by the host.

3) The signal should be tied to VCC by the host.

4) The mode is optional for CF+ Cards, but required for CompactFlash Storage Cards.

5) The -CSEL signal is ignored by the card in PC Card modes. However, because it is not pulled up on the card in these modes, it should not be left floating by the host in PC Card modes. In these modes, the pin should be connected by the host to PC Card A25 or grounded by the host.

6) If DMA operations are not used, the signal should be held high or tied to VCC by the host. For proper operation in older hosts: while DMA operations are not active, the card shall ignore this signal, including a floating condition

7) Signal usage in True IDE Mode except when Ultra DMA mode protocol is active.

8) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Write is active.

9) Signal usage in True IDE Mode when Ultra DMA mode protocol DMA Read is active.

## Signal Description:

# Compact Flash Card

(TCF80XXX)

TEKQ International

Signal Name	Dir.	Pin	Description
A10 - A0 (PC Card Memory Mode)	I	8,10,11,12, 14,15,16,17, 18,19,20	These address lines along with the -REG signal are used to select the following: The I/O port address registers within the CompactFlash Storage Card or CF+ Card, the memory mapped port address registers within the CompactFlash Storage Card or CF+ Card, a byte in the card's information structure and its configuration control and status registers.
A10 - A0 (PC Card I/O Mode)			This signal is the same as the PC Card Memory Mode signal.
A2 - A0 (True IDE Mode)	I	18,19,20	In True IDE Mode, only A[2:0] are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.
BVD1 (PC Card Memory Mode)	I/O	46	This signal is asserted high, as BVD1 is not supported.
-STSCHG (PC Card I/O Mode) Status Changed			This signal is asserted low to alert the host to changes in the READY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register.
-PDIAG (True IDE Mode)			In the True IDE Mode, this input / output is the Pass Diagnostic signal in the Master / Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	45	This signal is asserted high, as BVD2 is not supported.
-SPKR (PC Card I/O Mode)			This line is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated.
-DASP (True IDE Mode)			In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (PC Card Memory Mode)	O	26,25	These Card Detect pins are connected to ground on the CompactFlash Storage Card or CF+ Card. They are used by the host to determine that the CompactFlash Storage Card or CF+ Card is fully inserted into its socket.
-CD1, -CD2 (PC Card I/O Mode)			This signal is the same for all modes.
-CD1, -CD2 (True IDE Mode)			This signal is the same for all modes.
-CE1, -CE2 (PC Card Memory Mode) Card Enable	I	7,32	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0, -CE1, -CE2 allows 8 bit hosts to access all data on D0-D7. See Table 27, Table 29, Table 31, Table 35, Table 36 and Table 37.
-CE1, -CE2 (PC Card I/O Mode) Card Enable			This signal is the same as the PC Card Memory Mode signal.
-CS0, -CS1 (True IDE Mode)			In the True IDE Mode, -CS0 is the chip select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register.  While -DMACK is asserted, -CS0 and -CS1 shall be held negated and the width of the transfers shall be 16 bits.

# Compact Flash Card

(TCF80XXX)

TEKQ International

Signal Name	Dir.	Pin	Description
-CSEL (PC Card Memory Mode) -CSEL (PC Card I/O Mode) -CSEL (True IDE Mode)	I	39	<p>This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.</p> <p>This signal is not used for this mode, but should be connected by the host to PC Card A25 or grounded by the host.</p> <p>This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.</p>
D15 - D00 (PC Card Memory Mode) D15 - D00 (PC Card I/O Mode) D15 - D00 (True IDE Mode)	I/O	31,30,29,28, 27,49,48,47, 6,5,4,3,2, 23, 22, 21	<p>These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.</p> <p>This signal is the same as the PC Card Memory Mode signal.</p> <p>In True IDE Mode, all Task File operations occur in byte mode on the low order bus D[7:0] while all data transfers are 16 bit using D[15:0].</p>
GND (PC Card Memory Mode) GND (PC Card I/O Mode) GND (True IDE Mode)	--	1,50	<p>Ground.</p> <p>This signal is the same for all modes.</p> <p>This signal is the same for all modes.</p>
-INPACK (PC Card Memory Mode) -INPACK (PC Card I/O Mode) Input Acknowledge DMARQ (True IDE Mode)	O	43	<p>This signal is not used in this mode.</p> <p>The Input Acknowledge signal is asserted by the CompactFlash Storage Card or CF+ Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash Storage Card or CF+ Card and the CPU.</p> <p>This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by -IORD and -IOWR. This signal is used in a handshake manner with -DMACK, i.e., the device shall wait until the host asserts -DMACK before negating DMARQ, and re-asserting DMARQ if there is more data to transfer.</p> <p>DMARQ shall not be driven when the device is not selected.</p> <p>While a DMA operation is in progress, -CS0 and -CS1 shall be held negated and the width of the transfers shall be 16 bits.</p> <p>If there is no hardware support for DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device drivers will not attempt DMA mode.</p> <p>A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation in any mode.</p>
-IORD (PC Card Memory Mode)	I	34	<p>This signal is not used in this mode.</p>

# Compact Flash Card

(TCF80XXX)

TEKQ International

Signal Name	Dir.	Pin	Description
-IORD (PC Card I/O Mode)  -IORD (True IDE Mode – Except Ultra DMA Protocol Active)  -HDMARDY (True IDE Mode – In Ultra DMA Protocol DMA Read)  HSTROBE (True IDE Mode – In Ultra DMA Protocol DMA Write)			<p>This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash Storage Card or CF+ Card when the card is configured to use the I/O interface.</p> <p>In True IDE Mode, while Ultra DMA mode is not active, this signal has the same function as in PC Card I/O Mode.</p> <p>In True IDE Mode when Ultra DMA mode DMA Read is active, this signal is asserted by the host to indicate that the host is read to receive Ultra DMA data-in bursts. The host may negate -HDMARDY to pause an Ultra DMA transfer.</p> <p>In True IDE Mode when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the host. Both the rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.</p>
-IOWR (PC Card Memory Mode)  -IOWR (PC Card I/O Mode)    -IOWR (True IDE Mode – Except Ultra DMA Protocol Active)  STOP (True IDE Mode – Ultra DMA Protocol Active)	I	35	<p>This signal is not used in this mode.</p> <p>The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash Storage Card or CF+ Card controller registers when the CompactFlash Storage Card or CF+ Card is configured to use the I/O interface.</p> <p>The clocking shall occur on the negative to positive edge of the signal (trailing edge).</p> <p>In True IDE Mode, while Ultra DMA mode protocol is not active, this signal has the same function as in PC Card I/O Mode. When Ultra DMA mode protocol is supported, this signal must be negated before entering Ultra DMA mode protocol.</p> <p>In True IDE Mode, while Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst.</p>
-OE (PC Card Memory Mode)  -OE (PC Card I/O Mode)  -ATA SEL (True IDE Mode)	I	9	<p>This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Storage Card or CF+ Card in Memory Mode and to read the CIS and configuration registers.</p> <p>In PC Card I/O Mode, this signal is used to read the CIS and configuration registers.</p> <p>To enable True IDE Mode this input should be grounded by the host.</p>

Signal Name	Dir.	Pin	Description
READY (PC Card Memory Mode)	O	37	In Memory Mode, this signal is set high when the CompactFlash Storage Card or CF+ Card is ready to accept a new data transfer operation and is held low when the card is busy.  At power up and at Reset, the READY signal is held low (busy) until the CompactFlash Storage Card or CF+ Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Storage Card or CF+ Card during this time.  Note, however, that when a card is powered up and used with RESET continuously disconnected or asserted, the Reset function of the RESET pin is disabled. Consequently, the continuous assertion of RESET from the application of power shall not cause the READY signal to remain continuously in the busy state.
-IREQ (PC Card I/O Mode)			I/O Operation – After the CompactFlash Storage Card or CF+ Card has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE Mode)			In True IDE Mode signal is the active high Interrupt Request to the host.
-REG (PC Card Memory Mode) Attribute Memory Select	I	44	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.  The signal shall also be active (low) during I/O Cycles when the I/O address is on the Bus.
-DMACK (True IDE Mode)			This is a DMA Acknowledge signal that is asserted by the host in response to DMARQ to initiate DMA transfers.  While DMA operations are not active, the card shall ignore the -DMACK signal, including a floating condition.  If DMA operation is not supported by a True IDE Mode only host, this signal should be driven high or connected to VCC by the host.  A host that does not support DMA mode and implements both PCMCIA and True-IDE modes of operation need not alter the PCMCIA mode connections while in True-IDE mode as long as this does not prevent proper operation all modes.
RESET (PC Card Memory Mode)	I	41	The CompactFlash Storage Card or CF+ Card is Reset when the RESET pin is high with the following important exception:  The host may leave the RESET pin open or keep it continually high from the application of power without causing a continuous Reset of the card. Under either of these conditions, the card shall emerge from power-up having completed an initial Reset.  The CompactFlash Storage Card or CF+ Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set.  This signal is the same as the PC Card Memory Mode signal.
RESET (PC Card I/O Mode)			
-RESET (True IDE Mode)			In the True IDE Mode, this input pin is the active low hardware reset from the host.
VCC (PC Card Memory Mode)	--	13,38	+5 V, +3.3 V power.

# Compact Flash Card

(TCF80XXX)

TEKQ International

Signal Name	Dir.	Pin	Description
VCC (PC Card I/O Mode) VCC (True IDE Mode)			This signal is the same for all modes.  This signal is the same for all modes.
-VS1 -VS2 (PC Card Memory Mode)  -VS1 -VS2 (PC Card I/O Mode)  -VS1 -VS2 (True IDE Mode)	O	33 40	Voltage Sense Signals. -VS1 is grounded on the Card and sensed by the Host so that the CompactFlash Storage Card or CF+ Card CIS can be read at 3.3 volts and -VS2 is reserved by PCMCIA for a secondary voltage and is not connected on the Card.  This signal is the same for all modes.  This signal is the same for all modes.
-WAIT (PC Card Memory Mode)  -WAIT (PC Card I/O Mode)  IORDY (True IDE Mode – Except Ultra DMA Mode)  -DDMARDY (True IDE Mode – Ultra DMA Write Mode)  DSTROBE (True IDE Mode – Ultra DMA Read Mode)	O	42	The -WAIT signal is driven low by the CompactFlash Storage Card or CF+ Card to signal the host to delay completion of a memory or I/O cycle that is in progress.  This signal is the same as the PC Card Memory Mode signal.  In True IDE Mode, except in Ultra DMA modes, this output signal may be used as IORDY.  In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is asserted by the host to indicate that the device is read to receive Ultra DMA data-in bursts. The device may negate -DDMARDY to pause an Ultra DMA transfer.  In True IDE Mode, when Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-out burst.
-WE (PC Card Memory Mode)  -WE (PC Card I/O Mode)  -WE (True IDE Mode)	I	36	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Storage Card or CF+ Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers.  In PC Card I/O Mode, this signal is used for writing the configuration registers.  In True IDE Mode, this input signal is not used and should be connected to VCC by the host.
WP (PC Card Memory Mode) Write Protect  -IOIS16 (PC Card I/O Mode)  -IOCS16 (True IDE Mode)	O	24	Memory Mode – The CompactFlash Storage Card or CF+ Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.  I/O Operation – When the CompactFlash Storage Card or CF+ Card is configured for I/O Operation Pin 24 is used for the -I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.  In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

### DC Characteristic:

#### Absolute Maximum Ratings:

Symbol	Parameter	Rating	Units
V <sub>DD</sub>	Power supply	-0.3 to 6.0	V
V <sub>IN</sub>	Input voltage	-0.3 to V <sub>DD</sub> +0.3	V
V <sub>OUT</sub>	Output voltage	-0.3 to V <sub>DD</sub> +0.3	V
T <sub>STG</sub>	Storage temperature	-40 to 125	°C

#### Recommended Operating Conditions:

Symbol	Parameter	Min.	Max.	Units
V <sub>DD</sub>	Power supply	3.0	5.5	V
V <sub>IN</sub>	Input voltage	0	V <sub>DD</sub>	V
T <sub>OPR</sub>	Operating temperature	-20	65	°C

#### General DC Characteristics:

Sym.	Parameter	Conditions	Min	Typ	Max	Units
I <sub>IL</sub>	Input low current	no pull up/down	-1		1	μA
I <sub>IH</sub>	Input high current	no pull up/down	-1		1	μA
I <sub>OZ</sub>	Tri-state leakage current		-10		10	μA
C <sub>IN</sub>	Input capacitance			4		pF
C <sub>OUT</sub>	Output capacitance			4		pF
C <sub>BID</sub>	Bi-derection capacitance			4		pF

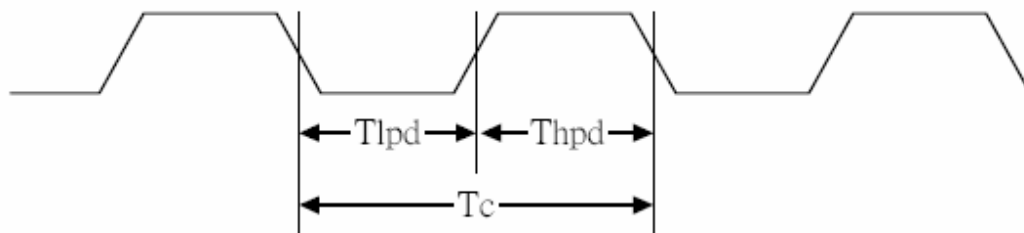
#### DC Electrical Characteristics:

Sym.	Parameter	Min	Typ	Max	Units
V <sub>IL</sub>	Input low voltage			0.3V <sub>DD</sub>	V
V <sub>IH</sub>	Input high voltage	0.7V <sub>DD</sub>			V
V <sub>IL</sub>	Schmitt input low voltage		1.22		V
V <sub>IH</sub>	Schmitt input high voltage		2.08		V
V <sub>OL</sub>	Output low voltage			0.4	V
V <sub>OH</sub>	Output high voltage	2.3		1	V
R <sub>I</sub>	Input pull up/down resistance		75		kΩ

## AC Characteristics:

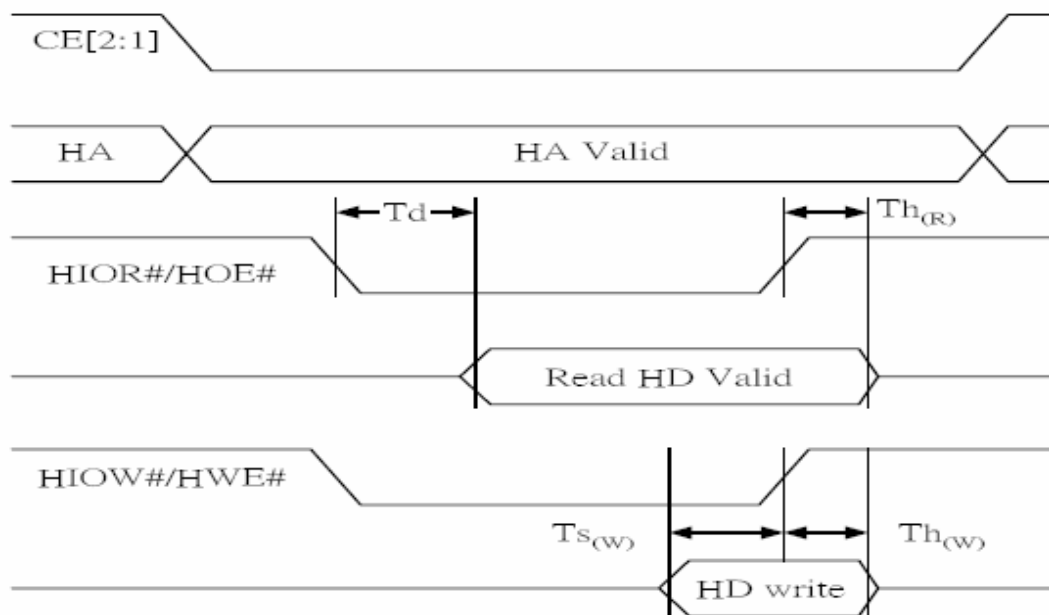
### System clock timing:

Sym.	Description	Min.	Typ.	Max.	Unit
Tc	Clock cycle time	45	50	100	ns
Tl <sub>pd</sub>	Clock low pulse duration	0.4Tc		0.6Tc	ns
Th <sub>pd</sub>	Clock high pulse duration	0.4Tc		0.6Tc	ns



### Host Read/Write timing:

Sym.	Description	Min.	Typ.	Max.	Unit
T <sub>d</sub>	HD bus asserted from HIOR# / HOE#			10	ns
Th <sub>(R)</sub>	HD hold time after HIOR# / HOE#	40		70	ns
T <sub>s(w)</sub>	HD set up time of HIOW# / HWE#	10			ns
Th <sub>(W)</sub>	HD hold time of HIOW# / HWE#	5			ns



Flash Read/Write timing:

Sym.	Description	Min.	Typ.	Max.	Unit
$T_{C(F)}$	Flash Read / Write cycle time		100		ns
$T_{S(FW)}$	FD set up time of FWE#	80			ns
$T_{H(FW)}$	FD hold time of FWE#	40			ns
$T_{S(FR)}$	FD set up time of FRD#	10			ns
$T_{H(FR)}$	FD hold time of FRD#	5			ns

